AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A data processing ~~device which reads out program instructions from an instruction region in a main memory and writes a result of a computation into the main memory,~~

~~the data processing device~~ apparatus for speeding-up execution of program instructions received from a main memory, comprising:

a main memory which stores program instructions and data;

a first instruction stream processor ~~including programmed logic circuitry~~ comprising a computing unit configured to perform computations based on one or more instructions ~~in the instruction region which are read out from the~~ obtained from an instruction region in main memory containing program instructions;

a register by which the first instruction stream processor writes and reads instruction data to/from the main ~~memory;~~ memory, and

an input/output group ~~generating programmed logic circuitry configured to generate an~~ generator, operatively functioning as an instruction sequence reuse window, that generates input/output (I/O) group ~~at a time of~~ data based on execution of ~~one or more~~ a sequence of program instructions ~~in~~ from the instruction region, said I/O group data having an input pattern comprising one or more instruction sequence input elements and an associated output pattern comprising one or more instruction sequence output elements; and

~~a memory, distinct from said main memory, having~~ said data processing apparatus further comprising an instruction region storage section comprising CAM and RAM memory portions,

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operatively functioning as data reuse table, ~~dedicated~~ for storing I/O group data used for reusing certain sequences of instructions, wherein said instruction region storage section further includes an I/O group storage portion used to store the I/O group data, and wherein ~~at the time of~~ ~~execution of~~, at a time of executing one or more instructions read out from the instruction region in main memory, and upon identifying a matching ~~an input~~ pattern ~~in~~ of instruction sequence input data found the instruction region with an input pattern ~~in the input/output~~ of I/O group data stored in the I/O group storage portion, the first stream processor performs a reuse operation that outputs the associated output pattern to the register and/or the main memory, and ~~further~~ wherein

~~the input/output group generating programmed logic circuitry includes a dependency~~ ~~relations storage memory section and also generates dependency relations information.~~ the input/output group generator also generates dependency relations information and includes a dependency relations storage memory section for storing dependency relations information, the dependency relations storage memory section comprising a two-dimensional (2D) matrix-arranged memory in which instruction sequence input elements are associated to particular columns of the memory and corresponding instruction sequence output elements are associated to particular rows of the memory, and each storage element within the 2D matrix-arranged memory contains dependency relations information indicative of whether a particular instruction sequence output element corresponding to a particular row of the memory is derived from or has some dependency relationship to a particular instruction sequence input element corresponding to a particular column of the memory, and wherein ~~which is stored in the dependency relations~~ ~~storage memory section, that identifies input values and input addresses, for a register/memory~~ ~~from which a readout operation is performed, corresponding to input elements in the input~~ ~~pattern of the input/output group from which each output value and output address, for a~~

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~~register/memory to which a writing operation is performed, corresponding to output elements in~~

~~an associated output pattern is derived; and~~

~~input/output group setting programmed logic circuitry configured~~

the input/output group generator further includes an I/O group data setter which, based on

information stored in the dependency relations ~~information, to set an input/output group~~ storage

memory, sets I/O group data that is made up of an output pattern ~~including~~ that includes at least

one of said instruction sequence output ~~element~~ elements and an input pattern ~~including~~ that

includes at least one of said instruction sequence input ~~element~~ elements.

2. (Currently amended) The data processing device as defined in claim 1, wherein if a

first group of instruction sequence input elements, from which a first instruction sequence output

element is derived, is included entirely within a second group of instruction sequence input

elements, from which a second instruction sequence output element different from the first

instruction sequence output element is derived, the ~~input/output group programmed logic~~

~~circuitry sets~~ I/O group data setter: (i) sets the second group of instruction sequence input

elements as the input pattern and (ii) sets the first group of instruction sequence input elements

and the second group of instruction sequence input elements as the output pattern.

3. (Currently amended) The data processing device as defined in claim 1, wherein if

there is no shared instruction sequence input element between a first group of instruction

sequence input elements, from which a first instruction sequence output element is derived, and a

second group of instruction sequence input elements, from which a second instruction sequence

output element different from the first instruction sequence output element is derived, the

input/output pattern group setting programmed logic circuitry sets I/O group data setter: (i) sets a

first input/output I/O group data in which the first group of the instruction sequence input

elements is the input pattern and the first instruction sequence output element is the output

pattern and (ii) sets a second input/output I/O group data in which the second group of the

instruction sequence input elements is the input pattern and the second instruction sequence

output element is the output pattern.

       Claim 4 (Canceled)

       5. (Currently amended) The data processing device as defined in claim 4, wherein after

a readout operation from the register and/or from an instruction region in the main memory is

performed when the and upon said first instruction stream processor performs a computation

based on performing execution of one or more instructions obtained from the register or the

instruction region, then the input/output group generating programmed logic circuitry generator

further performs operations of:

       (1) when an address of the register and/or the main memory from which the readout

operation was performed has been is registered in the dependency relations storage memory

section as an instruction sequence output element, temporarily storing creating a temporary

provisional dependency relationship information storage matrix comprising a row element of

rows and columns of memory elements within the dependency relations storage memory section,

wherein said a particular row element corresponds is associated to the that particular instruction

sequence output element corresponding to the registered address;

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(2) when an address of the register and/or the main memory from which the readout operation was performed is registered in the dependency relations storage memory section as an instruction sequence input element rather than an instruction sequence output element, temporarily storing a creating a temporary provisional dependency relationship information storage matrix in which a memory element corresponding to a column element of comprising rows and columns of memory elements within the dependency relations storage memory section, wherein said a particular column of memory elements is associated to that particular instruction sequence element corresponds to the input element corresponding to the registered address, and wherein said a particular memory element in a column element associated with the instruction sequence input element is set to a logical "1", and remaining memory elements in a same column are set to a logical "0"; and

(3) when an address of the register or the main memory from which the readout operation was performed is registered in the dependency relations storage section as neither an instruction sequence output element nor an instruction sequence input element, (i) registering, as input elements, the address and its value in the dependency relations storage section as instruction sequence input elements, and (ii) temporarily storing a provisional creating a temporary provisional dependency relationship information storage matrix in which a memory element corresponds to a column of comprising rows and columns of memory elements within the dependency relations storage memory section, wherein said a particular column corresponds of memory elements is associated to that particular instruction sequence registered as to the input element elements and a particular memory element in said column is set to a logical "1", and remaining memory elements in that same column are set to a logical "0"; and

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under a condition where a writing operation is performed to the register and/or the main

memory, the ~~input/output group generating programmed logic circuitry further performing~~ I/O

group data generator performs further operations of:

(4) when an address of the register and/or the main memory to which the writing

operation is performed is registered as an instruction sequence output element, (iii) updating an

instruction sequence output value corresponding to the registered instruction sequence output

element to ~~the~~ a value written by the writing operation ~~value~~, (iv) replacing a value stored in a

row element of the temporary provisional dependency relationship information storage matrix

within the dependency relations storage section, wherein said row element being replaced

corresponds to a row associated to the registered instruction sequence output element, with a

result of a logical ~~OR~~ OR-ing of all provisional matrices temporarily stored at that time, and then

(v) ~~then~~ initializing the temporarily-stored provisional matrices; and

(5) when an address of the register and/or the main memory means to which the writing

operation is performed is not registered as an instruction sequence output element, (vi)

registering the address and its value as an instruction sequence output element in the dependency

relations storage memory section, (vii) replacing a value stored in a row element of the

temporary provisional dependency relationship information storage matrix within the

dependency relations storage section, wherein said row element being replaced corresponds to a

row associated to that ~~the~~ instruction sequence output element, with a result of a logical ~~OR~~ OR-

ing of all provisional matrices temporarily stored at that time, and then (viii) ~~then~~ initializing the

temporarily-stored provisional matrices.

6. (Currently amended) The data processing device as defined in claim 4, wherein,

the ~~input/output group setting programmed logic circuitry~~ I/O group data pattern setter

includes a ~~rows "AND" operation comparison section~~ logical operation computation section

which performs a logical "AND" operation of the row elements in the 2D matrix-arranged

memory, and

~~in the dependency relations storage section, the input/output group setting programmed~~

~~logic circuitry~~ (i) extracts a group of row elements for which a logical AND operation of an

inversion of a first row element and a second row element are each a logical "0", and (ii) among

the extracted group of the row elements, excludes, ~~from~~ as a candidate ~~as the~~ for an input/output

group, row elements other than a row element that includes a largest number of the input

elements.

7. (Currently amended) The data processing device as defined in claim 4, wherein,

the ~~input/output group setting programmed logic circuitry~~ I/O group data pattern setter

includes a ~~rows AND comparison~~ logical operation computation section which performs a

logical "AND" operation of the row elements in the 2D matrix-arranged memory, and

~~in the dependency relations storage section, the input/output group setting programmed~~

~~logic circuitry~~ sets, as ~~the~~ an input/output group, a row element whose logical "AND" operation

with any other row elements are all ~~a~~ logical "0".

8. (Currently amended) The data processing device as defined in claim 1, further

comprising ~~at least one~~ a second instruction stream processor ~~including programmed logic~~

~~circuitry~~ having a second computing unit configured to perform computations on instructions ~~in the~~ from an instruction region in main memory,

wherein with respect to instructions in the instruction region processed by the first computing ~~means~~ unit, the second computing ~~means~~ unit subjects instructions ~~in~~ from the instruction region to a computation based on a predicted input value, and registers a result of the computation in the instruction region storage section.

9. (Currently amended) The data processing device as defined in claim 1, wherein,

the ~~input/output group setting programmed logic circuitry~~ I/O group data pattern setter further comprises:

an output-side group storage section which stores information of an input/output group to which each of the output elements belongs;

an input-side group storage section which stores information of an input/output group to which each of the input elements belongs;

a temporal storage section which stores a indication of a changed dependency relation between an output element and an input element whenever there is a change in information stored in the dependency relations storage section ~~while the input/output~~ when I/O group data is generated; and

a group temporal storage section which stores information of ~~a~~ changed ~~input/output~~ I/O group data when there is a change in information stored in the dependency relations storage memory section ~~while~~ when the input/output group is generated.

10. (Currently amended) The data processing device as defined in claim 9, wherein

the ~~input/output group setting programmed logic circuitry~~ I/O group data pattern setter

further includes a group management section that stores information of the ~~input/output~~ I/O

group data which has previously been allocated to ~~the~~ an output element and/or ~~the~~ an input

element ~~while~~ when the input/output group is ~~being~~ generated.

Claim 11 (Canceled)

12. (Currently amended) The data processing device as defined in claim ~~11~~ 10, wherein

the temporal storage section stores results of a logical ~~OR~~ OR-ing of memory elements of

a plurality of rows in the dependency relations storage section, and

the group temporal storage section stores: (i) the result of a logical ~~OR~~ OR-ing of

memory elements of a plurality of rows in the output side group storage section and/or (ii) the

result of a logical ~~OR~~ OR-ing of memory elements corresponding to a plurality of input elements

in the input side group storage section.

13. (Currently amended) The data processing device as defined in claim 9, wherein

the ~~input/output group setting programmed logic circuitry~~ I/O group data pattern setter

further includes a conditional branch storage section that stores information regarding an input

element on which the conditional branch instruction depends whenever a conditional branch

instruction is detected ~~while~~ when the ~~input/output~~ I/O group data is generated.

14. (Currently amended) The data processing device as defined in claim 12, wherein,

under a condition where a readout operation from the register and/or the main memory is

carried out while the first stream processor performs a calculation of the input region, the

input/output group ~~generating programmed logic circuitry~~ generator further performs operations

of:

(1) when an address of the register and/or the main memory from which the readout

operation was performed has been registered as an output element in the dependency relations

storage memory section, temporarily storing, in the temporal storage section, a logical OR of (i)

a row element of the dependency relations storage memory section, wherein said row element

corresponds to the output element, and (ii) elements in the temporal storage section, and storing,

in the group temporal storage section, a logical OR of (iii) a row element of the output side group

storage section, wherein said row element corresponds to the output element and (iv) elements in

the group temporal storage section;

(2) when an address of the register and/or the main memory from which the readout

operation was performed is registered as an input element rather than an output element in the

dependency relations storage memory section, storing in the temporal storage section

information in which a memory element corresponding to a column of the dependency relations

storage section, wherein said column corresponds to the input element and is set to a logical "1"

and remaining memory elements are set at a logical "0", and storing in the group temporal

storage section a logical "OR" of: (v) elements, from the input-side group storage section that

correspond to the input element and (vi) the elements in the group temporal storage section; and

(3) when an address of the register and/or the main memory from which the readout

operation was performed is not registered in the dependency relations storage memory section as

either an output element or an input element, registering as input elements, the address and its

value in the dependency relations storage section, and temporarily storing a provisional matrix in

which a memory element corresponding to a column, of the dependency relations storage

section, which corresponds to the input element is set at a logical "1" while remaining memory

elements are set to a logical "0", and

under a condition where writing is carried out to the register and/or the main memory, the

input/output group ~~generating programmed logic circuitry further~~ generator performs further

operations of:

(4) when an address of the register and/or the main memory to which the writing

performed is registered as an output element, updating an output value corresponding to the

registered output element to the written value, replacing a row element of the dependency

relations storage memory section wherein said row element corresponds to the registered output

element, with the information temporarily stored in the temporal storage section at the time, and

(viii) updating the information in the output side group storage section, which information

corresponds to the output element, and (ix) updating the information in the input side group

storage section, which information corresponds to the input elements on which the output

element depends, based on the information stored in the group temporal storage section; and

(5) when an address of the register and/or the main memory to which the writing is

carried out is not registered as an output element, registering the address and its value as output

element in the dependency relations storage memory section, and replacing a row element of the

dependency relations storage section, wherein said row element corresponds to the output

element, with the information temporarily stored in the temporal storage section at that time, and

(x) updating the information in the output-side group storage section, wherein said information

corresponds to the output element, and (xi) updating the information in the input side group

storage section, wherein said information corresponds to the input elements on which the output

element depends, based on the information stored in the group temporal storage section.

15. (Currently amended) The data processing device as defined in claim 1, wherein~

the instruction region storage section includes an instruction sequence input pattern

storage section which stores instruction sequence input patterns as a tree structure in which items

that are to which should be subjected to equal comparison are regarded as nodes.

16. (Currently amended) The data processing device as defined in claim 15, further

comprising wherein the input pattern storage programmed logic circuitry section is configured to

organize and store the tree structure in such a manner that a value of an item in the input pattern,

which item is subjected to equal comparison, is stored in association with an item which is to be

next subjected to a comparison.

17. (Currently amended) The data processing device as defined in claim 16, wherein~

the input pattern storage programmed logic circuitry section further includes associative

search performing programmed logic circuitry and an additional information storage section,

wherein the associative search performing programmed logic circuitry utilizes one or more

search target lines that include a value storage portion in which a value of an item to be subjected

to equal comparison is placed, and a key storage portion in which a key for identifying each item

is placed; and

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the additional information storage section includes a search item designation area in which an item to be next subjected to an associative search is stored in accordance with a search target line.

18.   (Withdrawn) A data processing device which reads out an instruction region from main memory means and writes a result of a computation into the main memory means,

the data processing device comprising:

first computing means for performing a computation based on the instruction region read out from the main memory means;

a register by which the first computing means reads out or writes data to/from the main memory means; and

input/output pattern storage means for storing an input pattern and an output pattern which are a result of execution of a plurality of instruction regions,

in a case where the first computing means executes an instruction region and an input pattern of the instruction region is matched with an input pattern stored in the input/output storage means, a reuse process is performed so that an output pattern, which is stored in the input/output storage means in association with the input pattern, is outputted to the register and/or the main memory means,

the data processing device further comprising:

registration processing means for (i) distinguishing, among the input elements in the input pattern, an input element to be subjected to prediction from an input element not requiring prediction, at the time of storing, in the input/output storage means, a result of execution of the

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instruction region by the first computing means, and (ii) registering, in the input/output storage

means, information regarding the distinction;

prediction processing means for predicting a variation of a value of the input element to

be subjected to prediction among the input elements stored in the input/output storage means,

based on the information regarding the distinction; and

second computing means for subjecting the instruction region to precomputation, based

on the input element predicted by the prediction processing means,

a result of the precomputation of the instruction region by the second computing means

being stored in the input/output storage means.

19. (Withdrawn) The data processing device as defined in claim 18, wherein,

in a case where (i) an address of the register used for input is used as a stack pointer or a

frame pointer or (ii) a writing instruction to the address is a constant setting instruction, the

registration processing means sets a constant flag in the address, as the information for the

distinction, while in a case where neither (i) or (ii) holds true, the registration processing means

resets a constant flag of the address.

20. (Withdrawn) The data processing device as defined in claim 18, wherein,

in a case where an input element is newly stored in the input/output storage means, the

registration processing means resets, as the information for the distinction, a change flag in an

address of the input element, while, in a case where, after the input element is stored in the

input/output storage means, a storing instruction is executed with respect to the address, the

registration processing means sets a change flag in the address.

21. (Withdrawn) The data processing device as defined in claim 19, wherein,

in a case where an input element is newly stored in the input/output storage means, the registration processing means resets, as the information for the distinction, a history flag in an address of the input element, while, in a case where, at the time of execution of a load instruction with respect to the address, the constant flag is set in a register address from which the address is generated, the registration processing means sets a history flag in the address.

22. (Withdrawn) The data processing device as defined in claim 21, wherein,

in a case where an input element is newly stored in the input/output storage means, the registration processing means resets, as the information for the distinction, a flag of an address of the input element, while, after the input element is stored in the input/output storage means, a storing instruction is executed with respect to the address, the registration processing means sets a change flag in the address, and

the prediction processing means performs prediction of a variation of an input element, as to an address in which the change flag and the history flag are set, among addresses of the input elements stored in the input/output storage means.

23. (Withdrawn) The data processing device as defined in claim 18, wherein,

the prediction processing means performs prediction of a variation of an input element, only as to an input element in which a variation of a value of the input element in the history is not 0, among the input elements stored in the input/output storage means.

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24. (Withdrawn) The data processing device as defined in claim 18, wherein,

when the result of execution of the instruction region by the first computing means is

stored in the input/output storage means, the registration processing means (i) distinguishes,

among the input elements in the input pattern, an input element to be subjected to prediction

from an input element not requiring prediction, (ii) registers information regarding the distinction

in the input/output storage means, (iii) counts how many times storing is carried out at the time

of execution of the instruction region, as to the output elements of the output pattern stored in the

input/output storage means, and (iv) store the counted value in the input/output storage means,

and

the second computing means (i) subjects the instruction region to precomputation, based

on the input element having been predicted by the prediction processing means, and (ii) performs

the precomputation of the instruction region by waiting for a time corresponding to the number

of times of storing performed with respect to the input element based on the counted value, and

then performing readout from the main memory.

25. (Withdrawn) The data processing device as defined in claim 24, wherein,

the input/output storage means includes an input/output storage area which temporarily

stores an input pattern and an output pattern which are the result of execution of the instruction

region by the first computing means, and

the input/output storage area includes a store counter which counts how many times the

storing is carried out with respect to each of the output elements.

26. (Withdrawn) The data processing device as defined in claim 25, wherein,

the input/output storage means includes a history storage area which stores a history of a

past result of execution of each instruction region subjected to computation by the first

computing means, and

the registration processing means (i) stores, in the history storage area, the result of

execution which is stored in the input/output storage area, and (ii) with respect to an input

element having an address identical with an address of an output element which is stored, in the

history storage area, as a result of execution of the last time, registers a store counter of a

corresponding directly-preceding output element, as a store counter of the input element.

27. (Withdrawn) The data processing device as defined in claim 26, wherein,

the input/output storage means includes a predicted value storage area which stores an

input element predicted by the prediction processing means, and

the prediction processing means subjects, to prediction, an input element whose value

consistently varies between execution histories, among the input elements stored in the history

storage area, and stores a result of the prediction in the predicted value storage area.

28. (Withdrawn) The data processing device as defined in claim 26, wherein,

the input/output storage means includes a waiting-required address storage area which

stores an input element that should be read out from the main memory after waiting for a time

corresponding to the number of times of the storing, and

with respect to an input element whose address in an execution histories does not change

and whose variation of a value between the execution histories is inconsistent, the prediction

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processing means stores, in the waiting-required address storage area, the store counter and a

waiting counter as a value based on a predicted distance.

29. (Withdrawn) The data processing device as defined in claim 26, wherein,

the input/output storage means includes a waiting-required address storage area which

stores an input element that should be read out from the main memory after waiting for a time

corresponding to the number of times of the storing, and

with respect to an input element whose address changes between execution histories and

values of changed addresses change on account of the storing, among the input elements stored

in the history storage area, the prediction processing means stores, in the waiting-required

address storage area, a waiting counter as a value based on the store counter.

Claims 30-31 (Canceled)

32. (New) A data processing apparatus for speeding-up execution of program

instructions read from a main memory, comprising:

a main memory which stores program instructions;

an instruction region/sequence storage section distinct from main memory and

comprising content addressable memory (CAM) and random access memory (RAM); and

at least one instruction stream processor comprising:

a computing unit that performs computation based on one or more instructions

obtained from an instruction region in main memory, and

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an instruction sequence reuse window unit that determines instruction sequence

dependency relationship information and produces instruction sequence I/O group data

sets for prospective reuse by the computing unit, wherein the instruction sequence reuse

window unit includes a dependency relation information storage memory comprising a

two-dimensional (2D) matrix-arranged array of memory elements;

wherein said CAM and RAM of the instruction region/sequence storage section form a reuse

table for storing and retrieving I/O group data sets for prospective reuse by the computing unit.